Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A control system, comprising:

a bus;

a master device connected to the bus and configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the bus during the address interval, and transmit or receive a command or data during the data interval; and

a plurality of slave devices connected to the bus and configured to detect commencement of the bus cycle, begin to sample the destination address from the bus ~~one or more~~ a plurality of clock cycles after commencement of the address interval, and transmit or receive a command or data during the data interval.

2. (original) The control system of claim 1, wherein the bus includes a plurality of redundant buses and the master device includes a plurality of redundant master devices, each of the redundant master devices controlling one of the redundant buses.

3. (original) The control system of claim 1, wherein the bus includes:

multiplexed address and data signal lines configured to transport address, data, and commands,

a cycle valid signal line configured to indicate a valid bus cycle, and

a data/address interval signal line configured to differentiate the data interval from the address interval.

4. (original) The control system of claim 3, wherein the bus further includes:

parity signal lines that aid in detecting failures in the multiplexed address and data signal lines, the cycle valid signal line, and the data/address interval signal line.

5. (original) The control system of claim 1, wherein the destination address corresponds to an address of one of the slave devices.

6. (original) The control system of claim 1, wherein the master device is further configured to commence a read or write cycle on the bus.

7. (original) The control system of claim 6, wherein during the data interval of the read cycle, one of the slave devices is configured to drive a command or data on the bus until completion of the bus cycle.

8. (original) The control system of claim 7, wherein the one slave device corresponds to the destination address sampled during the address interval.

9. (previously presented) The control system of claim 6, wherein during the data interval of the write cycle, one of the slave devices is configured to sample a command or data on the bus a predetermined amount of time after commencement of the data interval.

10. (previously presented) The control system of claim 9, wherein the predetermined amount of time is approximately 5 clock cycles.

11. (original) The control system of claim 6, wherein during the data interval of the read cycle, the master device is configured to cease driving the bus to permit one of the slave devices to drive data back to the master device.

12. (original) The control system of claim 6, wherein during the data interval of the write cycle, the master device is configured to transmit a command or data on the bus.

13. (original) The control system of claim 1, wherein the master device is further configured to transmit a read-back signal to a destination device, receive a reply to the read-back signal, and determine the integrity of the destination device based on the received reply.

14. (original) The control system of claim 13, wherein the destination device includes at least one of another master device and one of the slave devices.

15. (original) The control system of claim 13, wherein the destination device includes the master device.

16. (original) The control system of claim 1, wherein the control system is a network device, the master device is a controller of a routing engine, and the slave devices are controllers of a packet forwarding engine.

17. (previously presented) A method for using a redundant bus by a master device and a plurality of slave devices in a multi-master system, comprising:

commencing a bus cycle by the master device, the bus cycle including an address interval followed by a data interval;

providing, by the master device, a destination address on the bus during the address interval;

sampling, by the slave devices, the destination address on the bus a plurality of clock cycles after a start of the address interval;

commencing read and write cycles by the master device;

during the data interval of the read cycle, transmitting data to the master device by one of the slave devices that corresponds to the destination address; and

during the data interval of the write cycle, transmitting data from the master device to one of the slave devices that corresponds to the destination address.

18. (previously presented) The method of claim 17, further comprising:

during the data interval of the write cycle, sampling data on the bus, by one of the slave devices that corresponds to the destination address, a predetermined amount of time after a start of the data interval.

19. (previously presented) The method of claim 18, wherein the predetermined amount of time is 5 clock cycles.

20. (currently amended) The method of claim 17, wherein the ~~one or more~~ plurality of clock cycles include 5 clock cycles.

21. (previously presented) A bus, comprising:

multiplexed address and data signal lines, of the bus, configured to transport address, data, and commands;

a cycle valid signal line, of the bus, configured to indicate commencement of a bus cycle that includes an address interval and a data interval;

a data/address interval signal line, of the bus, configured to differentiate between the address interval and the data interval;

a read/write signal line, of the bus, configured to indicate commencement of read and write cycles; and

parity signal lines, of the bus, configured to provide parity information relating to the multiplexed address and data signal lines, the cycle valid signal line, the data/address interval signal line, and the read/write signal line.

22. (original) The bus of claim 21, wherein the parity signal lines transmit two bits, one of the bits provides parity over the multiplexed address and data signal lines and the other one of the bits provides parity over the cycle valid signal line, the data/address interval signal line, and the read/write signal line.

23. (previously presented) A device, comprising:

a plurality of redundant buses;

a plurality of redundant master controllers connected to corresponding ones of the buses, one of the master controllers being an active master and other ones of the master controllers being standby masters, the active master being configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the corresponding bus during the address interval, and transmit or receive a command or data during the data interval; and

a plurality of slave controllers connected to the bus and configured to detect commencement of the bus cycle, sample the destination address from the bus one or more clock cycles after commencement of the address interval, and transmit or receive a command or data during the data interval.

24. (previously presented) The device of claim 23, wherein the network device is a router.

25. (previously presented) The device of claim 24, wherein the redundant master controllers are redundant routing engines and the slave controllers are switching and forwarding modules.

26. (currently amended) A control system that includes a bus, comprising:

means, connected to the bus, for commencing a bus cycle on the bus, the bus cycle including an address interval followed by a data interval;

means, connected to the bus, for providing a destination address on the bus during the address interval;

means, connected to the bus, for sampling the destination address on the bus ~~one or more~~ a plurality of first clock cycles after a start of the address interval;

means, connected to the bus, for providing data on the bus during the data interval; and

means, connected to the bus, for sampling the data on the bus ~~one or more~~ a plurality of second clock cycles after a start of the data interval.

27. (original) A multi-master system, comprising:

a plurality of redundant buses;

a plurality of slave devices connected to the buses; and

at least first and second master devices connected to corresponding ones of the buses, the first master device being configured to transmit a read-back signal to a destination device, receive a reply to the read-back signal, and determine the integrity of the destination device based on the received reply.

28. (original) The multi-master system of claim 27, wherein the destination device includes at least one of the second master device and one of the slave devices.

29. (original) The multi-master system of claim 27, wherein the destination device includes the first master device.